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TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Application Number	10/098,659
Filing Date	March 12, 2002
First Named Inventor	Robert Kerr et al.
Art Unit	2825
Examiner Name	Calvin Lee
Attorney Docket Number	MI22-19897

Total Number of Pages in This Submission

ENCLOSURES (Check all that apply)

<input type="checkbox"/> Fee Transmittal Form	<input type="checkbox"/> Drawing(s)	<input type="checkbox"/> After Allowance Communication to a Technology Center (TC)
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<input type="checkbox"/> Response to Missing Parts/Incomplete Application	Remarks	
<input type="checkbox"/> Response to Missing Parts under 37 CFR 1.52 or 1.53	Additional Enclosure: Request for Certificate of Correction	

Patent No.: 6,790,663 B2
Issued: September 14, 2004

**Certificate
JAN 25 2005
of Correction**

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm or Individual	D. Brent Kenady, Reg. No. 40,045 Wells St. John, P.S.
Signature	
Date	1-13-05

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I hereby certify that this correspondence is being facsimile transmitted to the USPTO or deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, Washington, DC 20231 on this date: 1/14/2005

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent No. 6,790,663 B2
Patent Issue Date September 14, 2004
Application Serial No. 10/098,659
Filing Date March 12, 2002
Assignee Micron Technology, Inc.
Inventorship Robert Kerr et al.
Attorney's Docket No. MI22-1987
Title: Methods of Contacting Lines and Methods of Forming an Electrical
Contact in a Semiconductor Device

REQUEST FOR CERTIFICATE OF CORRECTION OF PATENT
FOR PTO MISTAKE (37 C.F.R. 1.322(a))

To: Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450
ATTN: Decision and Certificate of Correction
Branch of the Patent Issue Division

From: D. Brent Kenady (Tel. 509-624-4276; Fax 509-838-3424)
Wells St. John P.S.
601 W. First Avenue, Suite 1300
Spokane, WA 99201-3828

Sir:

It is hereby requested that a Certificate of Correction be issued with respect to Patent No. 6,790,663 B2, granted September 14, 2004, in accordance with the Certificate of Correction form attached hereto in duplicate.


The errors listed on the Certificate of Correction form were apparently incurred through the fault of the PTO as will be disclosed by the records of files in the Office.

Since this Certificate of Correction is being requested due to PTO errors, it is believed that no fee is due. However, in the event that a fee is required for issuance of this Certificate of Correction, please charge the fee specified under

37 C.F.R. § 1.20(a) to Deposit Account No. 23-0925. Please credit Deposit Account No. 23-0925 with any overpayment of the above fee.

Attached hereto, in duplicate is Form PTO-1050, with at least one copy being suitable for printing.

Dated: 1-13-05

Respectfully submitted,
By: 
D. Brent Kenady
Reg. No. 40,045

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 6,790,663 B2
DATED : September 14, 2004
INVENTOR(S) : Robert Kerr et al.

It is certified that errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Title Page 1, "**References Cited**", "OTHER PUBLICATIONS", please insert --Gray & Meyer, "Analysis and Design of Analog Integrated Circuits", Third Edition, John Wiley & Sons, Inc., 1993, pg. 169--.

Col. 2, line 65, please delete "array Diffusion" after "memory" and insert --array. Diffusion--.

Page
1 of 1

Mailing Address of Sender:
D. Brent Kenady
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Patent No. 6,790,663 B2

UNITED STATES PATENT AND TRADEMARK OFFICE

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Patent No. 6,790,663 B2

JAN 25 2005

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JAN 18 2005
PATENT & TRADEMARK OFFICE

U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE				ATTY. DOCKET NO. M122-1987		SERIAL NO. Filed Herewith		
LIST OF ART CITED BY APPLICANT (Use several sheets if necessary)				APPLICANT Robert Kerr et al.				
				FILING DATE Filed Herewith		GROUP Unknown		
U.S. PATENT DOCUMENTS								
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate	
CL	AA	5,206,187	04/93	Doan et al.	437	192		
	AB	5,731,610	03/98	Rhodes	257	309		
	AC	5,162,890	11/92	Butler	257	306		
		5,173,752	12/92	Motonami et al.	257	309		
	AE	5,272,367	12/93	Dennison et al.	257	306		
	AF	5,317,193	05/94	Watanabe	257	774		
	AG	5,444,003	08/95	Wang et al.	437	31		
	AH	5,510,648	04/96	Davies et al.	257	657		
	AI	5,547,892	08/96	Wuu et al.	437	52		
	AJ	5,552,620	09/96	Lu et al.	437	195		
CL	AK	5,612,240	03/97	Chang	437	44		
	AL							
FOREIGN PATENT DOCUMENTS								
		Document Number	Date	Country	Class	Subclass	Translation	
							Yes	No
	AM							
	AN							
	AO							
	AP							
	AQ							
OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, Etc.)								
CL	AR		Gray & Meyer, "Analysis and Design of Analog Integrated Circuits", Third Edition, John Wiley & Sons, Inc., 1993, pg. 169					
	AS							
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EXAMINER				DATE CONSIDERED				
calvin				5.4.04				
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